CLAIMS

What is claimed is:

1. A nonvolatile memory array, comprising:

a plurality of diffused horizontal source lines, parallel to and interspersed with parallel control gate lines; and

a diffused vertical source line which intersects plural ones of said diffused horizontal source lines, said diffused vertical source line being flanked by isolation structures;

wherein said horizontal source lines are electrically connected to said vertical source line by dopants implanted under said control gate lines.

2. The memory array of Claim 1, wherein said dopants comprise arsenic.

3. The memory array of Claim 1, wherein said control gate lines overlie respective floating gates.

4. The memory array of Claim 1, further comprising source contacts which are substantially in line with drain contacts.

5. The memory array of Claim 1, further comprising a source contact which is located within said diffused vertical source line, but not in said plurality of diffused horizontal source lines.

6. A non-volatile memory array, comprising:

a plurality of diffused horizontal source lines, parallel to and interspersed with parallel control gate lines; and

a diffused vertical source line which intersects plural ones of said diffused horizontal source lines, said diffused vertical source line being flanked by isolation structures, wherein said horizontal source lines are separated from said vertical source line by said control gate lines;

a plurality of drain contacts separated from respective ones of said horizontal source lines by a respective control gate line, said control gate line containing individual floating gates; and

a source contact which is located in said vertical source line and is substantially in line with ones of said drain contacts;

wherein said source contact is electrically connected to said horizontal source line by dopants implanted under said respective control gate lines.

7. The memory array of Claim 6, wherein said dopants comprise arsenic.

18. A method of fabricating a nonvolatile memory array, comprising the steps of:

(a.) forming substantially parallel isolation structures in proximity to a surface of a substantially monolithic semiconductor material, said isolation structures at least partially defining horizontal source lines and a vertical source line which intersects ones of said horizontal source lines;

(b.) forming a first conductive layer on said substantially monolithic body of semiconductor material;

(c.) etching said first conductive layer to define an edge of floating gate structures and to expose a portion of said semiconductor material in said vertical source line;

(d.) after step (c.), implanting dopants into said exposed portion of said vertical source line;

(e.) after step (d.), forming a second conductive layer overlying said first conductive layer;

(f.) etching said first and second layers to form floating gate and control gate structures which intersect said isolation structures.

19. The method of Claim 18, wherein said dopants comprises arsenic.

20. The method of Claim 18, wherein said step (c.) exposes substantially all of said vertical source line.

21. The method of Claim 18, wherein said step (c.) exposes only that portion of said vertical source line which will lie under said control gate structures.

12. The method of Claim 8, further comprising the step of:

(g.) forming a source contact which is located within said vertical source line, but not in said plurality of horizontal source lines.